The Institution of Engineers, Malaysia

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Talk on "Electronics Packaging and Interconnection is there a limit to miniaturisation?"

Organised by the Consulting Engineering Special Interest Group, IEM
BEM Approved CPD/PDP Hours: 2 Ref No. IEM19/PG/397/T

Date : **28th August 2019**
Time : **5.30 pm – 7.30 pm** *(Refreshments will be served at 5.00 pm)*
Venue : **Tan Sri Prof. Chin Fung Kee Auditorium, 3rd Floor Wisma IEM**
Speaker : ***Professor Ndy Ekere*** *(BEng, MSc, PhD, CEng, FIET, FAS, SFHEA)*

SYNOPSIS

The last fifty years have seen very dramatic changes in the electronics manufacturing industry, which has had a major impact on society. A recent Reuters study shows that the global automotive electronics market will generate revenue of US$515.02 billion by 2027 and expanding at CAGR of 6.98% in the 2019-2027 forecast periods. This rapid evolution of the electronics manufacturing industry is started with the invention of the transistor and printed circuit board (PCB) in the late 1940's, through the development of the integrated circuit in the late 1950's, to the introduction of very high density area array interconnect technologies in the 1990's. Although cost and reliability are very important drivers in this globally competitive industry, the demand for product miniaturisation to meet customer requirements continues to be the key manufacturing challenge. A major trend in the design of hand-held and pocket electronic consumer products is to minimise chip packaging size to meet product requirements in terms of weight and size. At the same time the number of connections (device input-output) to a PCB is increasing to match existing and new digital/communication applications. This pressure for further miniaturisation presents new manufacturing challenges to the industry, as well as the impetus for researching novel packaging and interconnection materials/processes for meeting the emerging product requirements. The question facing the global industry is – "What is the limit to miniaturisation?" Using case studies of his own research at the University of Salford, University of Greenwich and now University of Wolver Hampton, Professor Ekere will highlight the Microsystems assembly technologies that are currently being developed to meet 21st Century product requirements, the interconnection and assembly trends, and the industrial and international collaboration that is helping to keep the UK at the forefront of the research on the miniaturisation of electronics interconnection and packaging.

FEE ANNOUNCEMENT
(Effective: 1st October 2017)

Members:
(i) Registration Fee: No Charge
(ii) Administrative Fee:
(a) Online RM15
(b) Walk-In RM20

Non-Members:
(i) Registration Fee: RM50
(ii) Administrative Fee: RM20

- Limited seats are available on a "first come first served" basis (maximum 100 participants).
- To secure your seat, kindly register online at www.myiem.org.my

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BIODATA OF SPEAKER

Professor Ndy Ekere is a Professor of Manufacturing Engineering and heads the Electronics Manufacture Engineering Research Group (EMERG). He was appointed Lecturer in the Department of Production Engineering at Nottingham Trent University in 1988, and then joined the University of Salford a year later as a lecturer in Manufacturing Engineering, where he founded the Electronics Manufacturing Engineering Research Group (EMERG) in 1992.

He served as the Dean of Engineering at the University of Greenwich (2002 – 2012; Dean of School of Technology at University of Wolverhampton (2013 – 2013); and founding Dean of Faculty of Science and engineering at University of Wolverhampton (2013 – 2016); before returning to a Professorial role in August 2016.

The focus of the research work carried out by the EMERG is to identify, explore and develop suitable assembly and packaging technologies both to meet the challenges of miniaturisation facing the electronics industry and to support virtual development of new and low-cost electronic products. As the trend towards minimising chip packaging size and increasing chip I/O count continues, one of the key challenges facing industry is that of developing low cost assembly solutions based on using conventional equipment. The group worked closely with industrial partners to develop a low cost, high volume flip-chip assembly route based on the assembly of solder-bumped chips on organic substrates, and the use of lead-free materials for flip-chip applications, flux less soldering for MEMS, and new materials for MEMS interconnect (including soldering of Si-wafers to glass/Cu). As new materials emerge, and the industry incorporate many different assembly materials into the assembly process, it is also critical to be able to describe the interactions between materials and process parameters, and the accurate characterisation and modelling is an important pre-requisite to achieving high yield and reliability.

Ir. S. Vignaeswaran
Chairman
Consulting Engineering Special Interest Group, IEM