

DEVELOPMENT OF LOW NOISE, VARIABLE HIGH GAIN AMPLIFIER FOR SIGNAL CONDITIONING CIRCUIT

Tan Chee Leong and Pukhraj Vaya

School of Engineering and Information Technology,
 University Malaysia Sabah, 88999 Kota Kinabalu, Sabah
 E-mail: vaya@ums.edu.my

ABSTRACT

This paper presents the design of low noise, variable high gain amplifier for signal conditioning circuit. A cascaded amplifier is used to improve the gain. A variable resistor is used to adjust the Common Mode Rejection Ratio (CMRR). The proposed amplifier is built on PCB board. Simulation and experimental results are discussed and compared. The new instrumentation amplifier has the features like gain up to 10000.0 gain, high linearity, and 106dB CMRR. It also has a low slew rate (0.07 V/ s) and wide gain bandwidth product (0.324 X10⁸Hz).

Keywords: Amplifier, CMRR, High Gain, Signal Conditioning Circuit

1. INTRODUCTION

A signal conditioning circuit is needed to amplify weak signal coming out of the sensor without any distortion. It is desirable that signal conditioning circuit has low signal to noise ratio with high CMRR and variable high gain. The amplifiers most commonly used for this purpose are i) differential amplifier [1], ii) bipolar transistor amplifier [2] and, iii) current

mode and voltage mode instrumentation amplifier [3]. A typical available instrumentation amplifier has CMRR = 80 dB and gain bandwidth = 1.5 MHz [4]. Instrumentation amplifier of Charles Kitchin and Lew Counts is used as basic circuit for development of a new instrumentation amplifier in the present study [4]. It provides a variable high gain, low noise, high input impedance and minimises the input bias current.

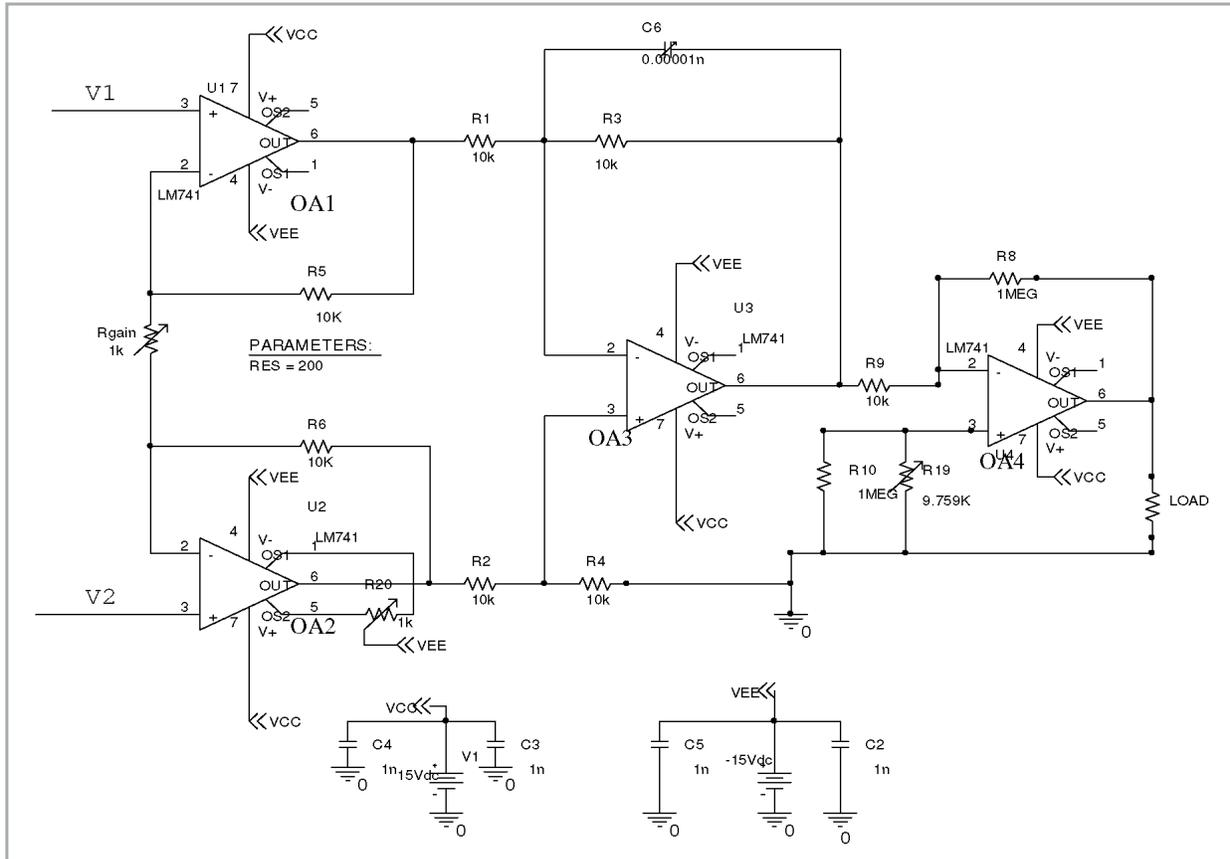


Figure 1: Modified low noise instrumentation amplifier with variable high gain

Instrumentation amplifier consists of three op-amps. 2 Op-amps are used for amplification and as input buffers; whereas another one is used as a differential amplifier rejecting the common mode signal. The variable resistor is used for gain adjustment. However this circuit has few limitations. The gain of the amplifier cannot exceed 10000.0 for DC amplification. It is due to the amplification limit of the operational amplifier used in the circuit. The instrumentation amplifier also has mismatching of resistances in the circuit due to inherent tolerances of the resistors. This degrades the CMRR of the amplifier. These problems are addressed in the design of our new amplifier circuit.

2. PROPOSED AMPLIFIER CIRCUIT

To improve the range of the gain and CMRR, modification were made on the basic instrumentation amplifier circuit as shown in Figure 1.

A cascaded differential amplifier OA4 is used to raise the gain up to 10000.0. It also reduces the nonlinearity. The gain expression for the modified circuits is given as:

$$A_v = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{2.R5}{R_{gain}}\right) \left(\frac{R8}{R9}\right) \quad (1)$$

where:

$$R1=R2=R3=R4, R5=R6, R8=R10 \text{ and } R9=R19$$

The total DC CMRR of the instrumentation amplifier is given in Equation 2 [5].

$$\frac{1}{CMRR_{Total}} = \frac{1}{CMRR_{IN}} + \frac{1}{CMRR_{CA}} \quad (2)$$

Where the subscripts $_{IN}$ and $_{CA}$ are used for instrumentation amplifier and cascaded amplifier respectively, $CMRR_{IN}$ and $CMRR_{CA}$ can be expressed [6]:

$$CMRR_{IN} = 20 \log \frac{gain_{IN}}{\frac{R3 + R1}{R1} = \frac{R2}{R2 + R4} - \frac{R3}{R1}} \quad (3)$$

$$CMRR_{CA} = 20 \log \frac{gain_{CA}}{1 - \frac{R8}{R19} \frac{R9}{R10}} \quad (4)$$

Equation 2 shows that one of the DC CMRR stages will dominate the total DC CMRR if it is much smaller than that of the other stage. We can control the DC CMRR of the modified instrumentation amplifier by using only one variable resistor. The variable resistor R19 is implemented in Figure 1. This maximises the CMRR of the cascaded amplifier stage. Variable Capacitor C6 is used to maximise the AC CMRR. The modifications in the circuit are also aimed at reducing the noise in the amplifier. A conventional offset trimming is used to minimise the offset noise [7]. The capacitors C2, C3, C4 and C5 are used to decouple the power supply. Decoupling is needed to assure that the noise current flows through the low impedance

bypass element rather than through the power supply [8]. The capacitors are also used as low pass filters for the high frequency content of any current that does pass through the series element, this make the power supply stable [8].

A prototype of the proposed amplifier is built on PCB board. This helps in minimising the noise in the circuit. The PCB layout is designed using Easy-PC software and developed using standard etching technique. Figure 2 shows the prototype of the amplifier.

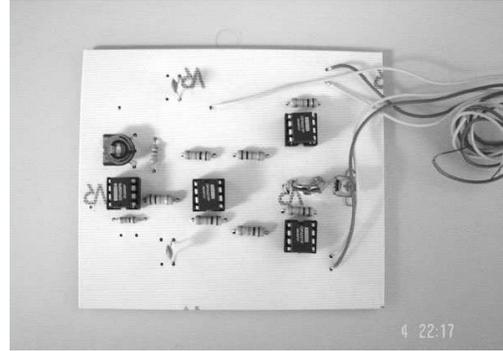


Figure 2: Prototype of the new amplifier

3. RESULTS AND DISCUSSION

Experimental verification of the new amplifier has been carried out by using the prototype amplifier. The gain of the circuit can be varied by adjusting the value of R1. The effects of variable resistor R19 and variable capacitor C6 on CMRR are studied and compared with the simulated results. Simulation was performed using circuit simulator PSPICE, the details of which are given in ref [9]. Figure 3 shows that the amplifier operates linearly even beyond the gain of 10000.0. Figure 4 shows the dependence of CMRR on R19. The discrepancy between the experimental and simulated results is due to the tolerance of components used in the prototype circuit. The sharp rise in simulated CMRR value is due to the impedance matching condition at R19 = 9.75K Ohm. Figure 5 shows that both experimental and simulated values of CMRR decrease exponentially with input frequency. The maximum value of 106 dB is obtained experimentally when R19 is kept constant at 9.75K Ohms. This discrepancy in the results is also attributed to the tolerance of the components and thermal instability. The DC CMRR remains unchanged for the entire range of amplifier gain (Figure 6). The gain bandwidth product of the amplifier is as high as 0.324×10^8 Hz.

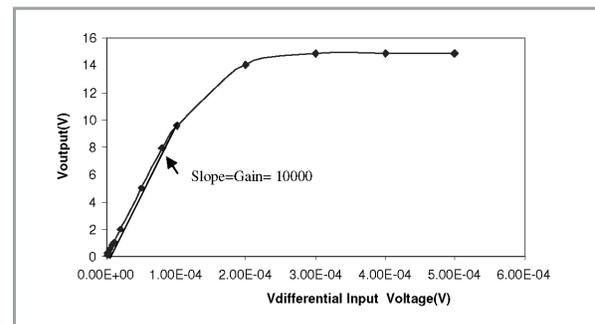


Figure 3: Linearity of the amplifier

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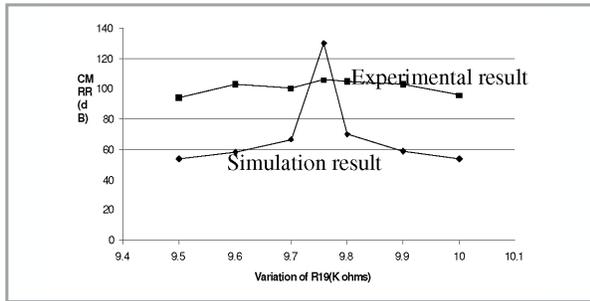


Figure 4: CMRR variation with respect to R19

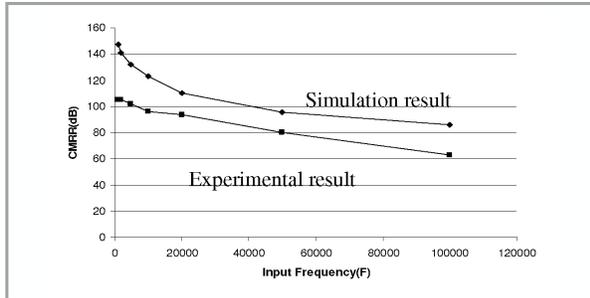


Figure 5: CMRR variation with respect to input frequency (R19 = 9.75K Ohms)

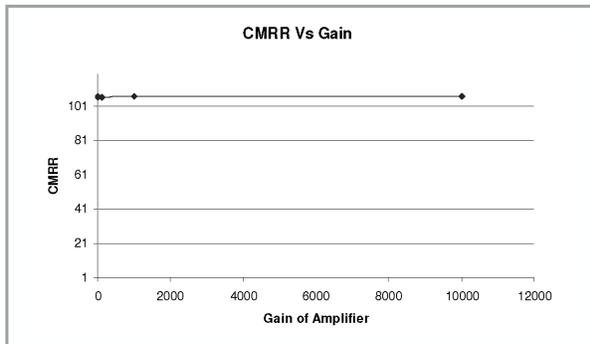


Figure 6: CMRR versus the Gain Range (R19 = 9.75K Ohms)

Slew rate of the proposed amplifier is also tested. Figure 7 show that the propose amplifier has slew rate as low as 0.07 V/ s.

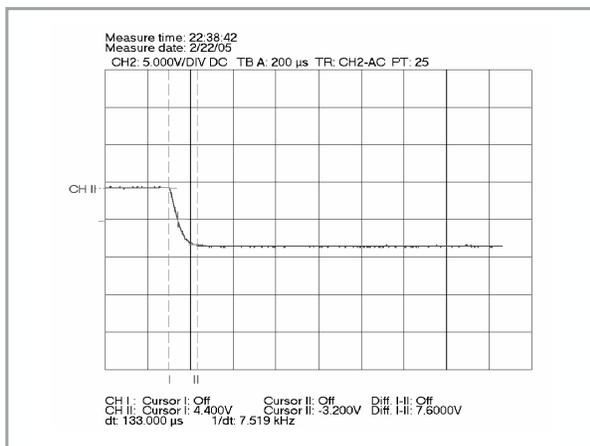


Figure 7: Slew rate experimental results

4. CONCLUSION

A low noise variable high gain instrumentation amplifier has been designed by using cascaded differential amplifier. The main advantages of this amplifier are a high variable gain (>10000gain) at minimum noise and high CMRR(106dB). The AC and DC CMRR can be maximised by using a variable capacitor and a variable resistor. This amplifier also has a wide gain bandwidth product compared to other amplifier. ■

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PROFILES



Tan Chee Leong was born in 1981 in Kuala Lumpur, Malaysia. He received his B.Sc in Electrical and Electronic Engineering from University Sabah Malaysia in 2005. His final year project was on "Signal Conditioning Circuitry for Thin Film Strain Gauges Sensor". Currently he is working for M.Sc degree in University Malaysia Sabah. His M.Sc project is modeling of semiconductor lasers. He has presented three conference papers and one research publication is under review. His main research interests are: characterization, modeling and fabrication of Quantum Well Laser, Vertical Cavity Laser and Optical Switching Devices.



Prof. Pukhraj Vaya is currently working as a Professor of Microelectronics, at Universiti Malaysia Sabah. He received M.Sc in Physics in 1966 from The University of Udaipur (India) and another M.Sc in Technology Degree in 1969 from Birla Institute of Technology and Science, Pilani (India). He was awarded PhD degree in electrical engineering, Indian Institute of Technology, Madras (India). He served the Department of Electrical Engineering, Indian Institute of Technology Madras (India) for 30 years. He has done extensive research and development work in the areas of both microelectronic and photonic devices. Prof. Vaya has many visiting assignments to credit. He was visiting fellow at The University of Singapore, Research Professor at the University of Illinois Chicago (UIC), USA, visiting Faculty at the University of Maryland Baltimore County (UMBC), USA, and visiting research fellow at University of New Castle, Australia. Prof. Vaya is a recipient of German DAAD short-term fellowship, senior associate of International Center for Theoretical Physics, Italy. He has traveled widely to many countries for scientific interactions. They include- USA, England, Canada, Germany, Italy, Yugoslavia, Republic of China, etc. He has produced more than 180 research papers, 3 industrial patents and edited 6 books/proceedings, organized many international conferences and short courses in the area of semiconductor device and technology. His current research interests include semiconductor materials, devices and technology, design and development of optoelectronic devices, MBE and MOCVD of III-V compounds, quantum well structures, sensors, modeling of photonic devices, scanning tunneling microscopy and nanofabrication using STM.